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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Date Submitted: February 18, 2004 (use as many sheets as necessary)				Application Number	Unassigned
				Filing Date	February 18, 2004
				First Named Inventor	Kedar PATEL et al.
				Group Art Unit	Unassigned
				Examiner Name	Unassigned
Sheet	1	of	15	Attorney Docket Number	035905-0134

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
TTN	A1	5,427,979		Chang	6/27/1995	
	A2	5,070,384		McCollum et al.	12/3/1991	
	A3	4,498,226		Inoue et al.	2/12/1985	
	A4	4,489,478		Sakurai	12/25/1984	
	A5	4,272,880		Pashley	6/16/1981	
	A6	5,745,407		Levy et al.	4/28/1998	
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	A11	4,543,594		Mohsen et al.	9/24/1985	
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	A13	4,646,266		Ovshinsky et al.	2/24/1987	
	A14	4,820,657		Hughes et al.	4/11/1989	
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	A19	3,990,098		Mastrangelo	11/2/1976	
	A20	4,146,902		Tanimoto et al.	3/27/1979	
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	A30	5,311,039		Kimura et al.	5/10/1994	
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Examiner Signature		Date Considered	10/17/2004
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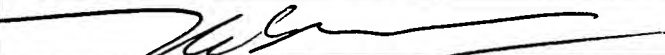
⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 18 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

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U.S. PATENT DOCUMENTS					
		U.S. Patent Document			
TTN	A43	3,571,809	Nelson	3/23/1971	
	A44	3,573,757	Adams	4/6/1971	
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	A46	3,846,767	Cohen	11/5/1974	
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	A49	3,922,648	Buckley	11/25/1975	
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	A67	5,306,935	Esquivel et al.	4/26/1994	
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	A87	4,630,096	Drye		
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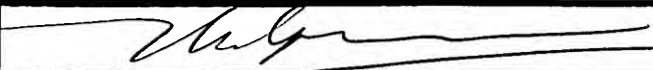
⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

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				Examiner Name	Unassigned
Sheet	3	of	15	Attorney Docket Number	035905-0134

U.S. PATENT DOCUMENTS					
	U.S. Patent Document				
15N	A89	4,710,798		Marcantonio	
	A90	4,811,082		Jacobs	
	A91	5,001,539		Inoue et al.	
	A92	5,089,862		Wamer, Jr. et al.	
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	A94	5,191,405		Tomita et al.	
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	A116	5,654,220		Leedy	
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	A123	5,915,167		Leedy	
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	A126	5,985,693		Leedy	
	A127	6,057,598		Payne et al.	
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15N	A134	6,307,257	B1	Huan et al.	

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U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Documents	Date of Publication of Cited Document MM-DD-YYYY
TN	A135	6,314,013	B1	Ahn et al.	
	A136	6,322,903	B1	Siniaguine et al.	
	A137	6,337,521	B1	Masuda	
	A138	6,353,265	B1	Michii	
	A139	6,355,501	B1	Fung et al.	
	A140	6,197,641	B1	Hergenrother et al.	

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Examiner Initials*	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Documents	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
TN	A141	EPO	0 073 486	A2	Toyama et al.	8-26-1982	
	A142	JP	61-222216		Takao	10-2-1986	
	A143	WO	94/26083		Carson et al.	11-10-1994	
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	A150	JP	63-52463		Hitachi Ltd	3-5-1998	
	A151	JP	6-22352		Fujitsu Ltd.	1-29-1994	
	A152	WO	02/15277	A2	Lee, et al.	2-21-02	

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS				
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.		
TN	A153	JOHN H. DOUGLAS: "The Route to 3-D Chips," High Technology, September 1983, pgs. 55-59, Vol. 3, No. 9, High Technology Publishing Corporation, Boston, MA		
TN	A154	M. ARIENZO et al.: "Diffusion of Arsenic in Bilayer Polycrystalline Silicon Films," J. Appl. Phys., January 1984, pgs. 365-369, Vol. 55, No. 2, American Institute of Physics		
TN	A155	O. BELLEZZA et al.: "A New Self-Aligned Field Oxide Cell for Multimegabit Eeproms," IEDM, pgs. 579-582, IEEE		
TN	A156	S.D. BROTHERTON et al.: "Excimer-Laser-Annealed Poly-Si Thin-Film Transistors," IEEE Transactions on Electron Devices, February 1993, pgs. 407-413, Vol. 40, No. 2, IEEE		
TN	A157	P. CANDELIER et al.: "Simplified 0.35-μm Flash EEPROM Process Using High-Temperature Oxide (HTO) Deposited by LPCVD as Interpoly Dielectrics and Peripheral Transistors Gate Oxide," IEEE Electron Device Letters, July 1997, pgs. 306-308, Vol. 18, No. 7, IEEE		

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TN	A158	MIN CAO et al.: "A High-Performance Polysilicon Thin-Film Transistor Using XeCl Excimer Laser Crystallization of Pre-Patterned Amorphous Si Films," IEEE Transactions on Electron Devices, April 1996, pgs. 561-567, Vol. 43, No. 4, IEEE		Y
TN	A159	MINO CAO et al.: "A Simple EEPROM Cell Using Twin Polysilicon Thin Film Transistors," IEEE Electron Device Letters, August 1994, pgs. 304-306, Vol. 15, No. 8, IEEE		Y
TN	A160	BOMY CHEN et al.: "Yield Improvement for a 3.5-ns BICMOS Technology in a 200-mm Manufacturing Line," IBM Technology Products, 1993, pgs.301-305, VLSITSA		Y
TN	A161	VICTOR W.C. CHAN et al.: "Three Dimensional CMOS Integrated Circuits on Large Grain Polysilicon Films," IEDM, 2000, IEEE		Y
TN	A162	BOAZ EITAN et al.: "Alternate Metal Virtual Ground (AMG) - A New Scaling Concept for Very High-Density EPROM's," IEEE Electron Device Letters, pgs. 450-452, Vol. 12, No. 8, August 1991, IEEE		Y
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TN	A164	DR. HEINRICH ENDERT: "Excimer Lasers as Tools for Material Processing in Manufacturing," Technical Digest: International Electron Devices Meeting, 1985, pgs. 28-29, Washington, DC, December 1-4, 1985, Göttingen, Germany		Y
TN	A165	DOV FROHMAN-BENTCHKOWSKY: "A Fully Decoded 2048-Bit Electrically Programmable FAMOS Read-Only Memory," IEEE Journal of Solid-State Circuits, pgs. 301-306, Vol. sc-6, No. 5, October 1971		Y
TN	A166	G.K. GIUST et al.: "Laser-Processed Thin-Film Transistors Fabricated from Sputtered Amorphous-Silicon Films," IEEE Transactions on Electron Devices, pgs. 207-213, Vol. 47, No. 1, January 2000, IEEE		Y
TN	A167	G.K. GIUST et al.: "High-Performance Thin-Film Transistors Fabricated Using Excimer Laser Processing and Grain Engineering," IEEE Transactions on Electron Devices, pgs. 925-932, Vol. 45, No. 4, April 1998, IEEE		Y
TN	A168	G.K. GIUST et al.: "High-Performance Laser-Processed Polysilicon Thin-Film Transistors," IEE Electron Device Letters, pgs. 77-79, Vol. 20, No. 2, February 1999, IEEE		Y

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TDN	A169	FUMIHIKO HAYASHI et al.: "A Self-Aligned Split-Gate Flash EEPROM Cell with 3-D Pillar Structure," 1999 Symposium on VLSI Technology Digest of Technical Papers, pgs. 87-88, Stanford University, Stanford, CA 94305, USA		Y
TDN	A170	STEPHEN C.H. HO et al.: "Thermal Stability of Nickel Silicides in Different Silicon Substrates," Department of Electrical and Electronic Engineering, pgs. 105-108, 1998, IEEE		Y
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TDN	A172	R. KAZEROUNIAN et al.: Alternate Metal Virtual Ground EPROM Array Implemented in a 0.8µm Process for Very High Density Applications," IEDM 91, pgs. 311-314, 1991, IEEE		Y
TDN	A173	CHANG-DONG KIM et al.: "Short-Channel Amorphous-Silicon Thin-Film Transistors," IEEE Transactions on Electron Devices, pgs. 2172-2176, Vol. 43, No. 12, December 1996, IEEE		Y
TDN	A174	JOHAN H. KLOOTWIJK et al.: "Deposited Inter-Polysilicon Dielectrics for Nonvolatile Memories," IEEE Transactions on Electron Devices, pgs. 1435-1445, Vol. 46, No. 7, July 1999, IEEE		Y
TDN	A175	WEB PAGE: JA-HUM KU et al.: "High Performance pMOSFETs With Ni(Si/sub x/Ge/sub 1-x Si/Sub 0.8/Ge/sub 0.2/ gate, IEEE Xplore Citation Web Page," VLSI Technology, 2000		Y
TDN	A176	NAE-IN LEE et al.: "High-Performance EEPROM's Using N- and P-Channel Polysilicon Thin-Film Transistors with Electron Cyclotron Resonance N2O-Plasma Oxide," pgs. 15-17, IEEE Electron Device Letters, Vol. 20, No. 1, January 1999, IEEE		Y
TDN	A177	JIN-WOO LEE et al.: "Improved Stability of Polysilicon Thin-Film Transistors under Self-Heating and High Endurance EEPROM Cells for Systems-On-Panel," IEEE Electron Device Letters, 1998, pgs. 265-268, IEEE		Y

Examiner Signature		Date Considered	10/17/2004
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Date Submitted: February 18, 2004 (use as many sheets as necessary)				Application Number	Unassigned
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				First Named Inventor	Kedar PATEL et al.
				Group Art Unit	Unassigned
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Sheet	7	of	15	Attorney Docket Number	035905-0134

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS				
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TDN	A178	SEOK-WOON LEE et al.: "Pd induced lateral crystallization of Amorphous Si Thin Films," Appl. Phys. Lett. 66 (13), pgs. 1671-1673, 27 March 1995, American Institute of Physics		Y
TDN	A179	K. MIYASHITA et al.: "Optimized Halo Structure for 80 nm Physical Gate CMOS Technology with Indium and Antimony Highly Angled Ion Implantation," IEDM 99-645, pgs. 27.2.1-27.2.4, 1999, IEEE		Y
TDN	A180	N.D. YOUNG et al.: "The Fabrication and Characterization of EEPROM Arrays on Glass Using a Low-Temperature Poly-Si TFT Process," IEEE Transactions on Electron Devices, pgs. 1930-1936, Vol. 43, No. 11, November 1996, IEEE		Y
TDN	A181	JUNG-HOON OH et al.: "A High-Endurance Low-Temperature Polysilicon Thin-Film Transistor EEPROM Cell," pgs. 304-306, IEEE Electron Device Letters, Vol. 21, No. 6, June 2000, IEEE		Y
TDN	A182	WEB PAGE: M.C. POON, et al.: "Thermal Stability of Cobalt and Nickel Silicides in Amorpho Crystalline Silicon," IEEE Xplore Web Page, 1997		Y
TDN	A183	NORIAKI SATO et al.: "A New Programmable Cell Utilizing Insulator Breakdown," IEDM 85, pgs. 639-642, 1985, IEEE		Y
TDN	A184	TAKEO SHIBA et al.: "In Situ Phosphorus-Doped Polysilicon Emitter Technology for Very High-Speed, Small Emitter Bipolar Transistors," IEEE Transactions on Electron Devices, pgs. 889-897, Vol. 43, No. 6, June 1996, IEEE		Y
TDN	A185	SEUNGHEON SONG et al.: "High Performance Transistors with State-of-the-Art CMOS Technologies," IEDM 99, pgs. 427-430, 1999, IEEE		Y
TDN	A186	YOSHIHIRO TAKAO et al.: "Low-Power and High-Stability SRAM Technology Using a Laser-Recrystallized p-Channel SOI MOSFET," IEEE Transactions on Electron Devices, pgs. 2147-2152, Vol. 39, No. 9, September 1992, IEEE		Y

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TON	A187	KENJI TANIGUCHI et al.: "Process Modeling and Simulation: Boundary Conditions for Point Defect-Based Impurity Diffusion Model," IEEE Transactions on Computer-Aided Design, pgs. 1177-1183, Vol. 9, No. 11, November 1990, IEEE		Y
TON	A188	HONGMEI WANG et al.: "Submicron Super TFTs for 3-D VLSI Applications," IEEE Electron Device Letters, Vol. 21, No. 9, pgs. 439-441, September 2000, IEEE		Y
TON	A189	HONGMEI WANG et al.: "Super Thin-Film Transistor with SOI CMOS Performance Formed by a Novel Grain Enhancement Method," IEEE Transactions on Electron Devices, pgs. 1580-1586, Vol. 47, No. 8, August 2000, IEEE		Y
TON	A190	MARVIN H. WHITE et al.: "On the Go With Sonos," Circuit & Devices, pgs. 22-31, July 2000, IEEE		Y
TON	A191	B.J. WOO et al.: "A Novel Memory Cell Using Flash Array Contactless Eprom (Face) Technology," IEDM, pgs. 90-93, 1990, IEEE		Y
TON	A192	WEB PAGE: QI XIANG et al.: "Deep sub-100 nm CMOS with Ultra Low Gate Sheet Resista NiSi," IEEE Xplore Web Page, 2000		Y
TON	A193	QI XIANG et al.: "Deep Sub-100nm CMOS with Ultra Low Gate Sheet Resistance by NiSi," IEEE, pgs. 76-77, 2000, Symposium on VLSI Technology Digest of Technical Papers		Y
TON	A194	QIUXIA XU et al.: "New Ti-SALICIDE Process Using Sb and Ge Preamorphization for Sub-0.2 μ m CMOS Technology," IEEE Transactions on Electron Devices, pgs. 2002-2009, Vol. 45, No. 9, September 1998, IEEE		Y
TON	A195	KUNIYOSHI YOSHIKAWA et al.: "An Asymmetrical Lightly Doped Source Cell for Virtual Ground High-Density EPROM's," IEEE Transactions on Electron Devices, pgs. 1046-1051, Vol. 37, No. 4, April 1990, IEEE		Y
TON	A196	VIVEK SUBRAMANIAN: "Control of Nucleation and Grain Growth in Solid-Phase Crystallized Silicon for High-Performance Thin Film Transistors," A Dissertation submitted to the Department of Electrical Engineering and the Committee of Graduate Studies of Stanford University, 1998		Y

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TDN	A197	DIETMAR GOGL et al.: "A 1-Kbit EEPROM in SIMOX Technology for High-Temperature Applications up to 250° C," IEEE Journal of Solid-State Circuits, October 2000, Vol. 35, No. 10, IEEE	Y
TDN	A198	BRIAN DIPERT: "Exotic Memories, Diverse Approaches: Newfangled Memory Technologies Come and Go, But Every Once in a While, One Makes It Out of the Laboratory and Into Your Next Design. All of These Candidates Aspire to be the Next Semiconductor Success Story. Which Ones' Dreams Will Come True?" EDN ASIA web page (September 2001)	Y
TDN	A199	ABOU-SAMRA S.J.: "3D CMOS SOI for High Performance Computing", Low Power Electronics and Design Proceedings, 1998.	Y
TDN	A200	YAMAZAKI K.: "4-Layer 3-D IC Technologies for Parallel Signal Processing", International Electron Devices Meeting Technical Digest, December 9-12, 1990, pgs 25.5.1 - 25.5.4.	Y
TDN	A201	AKASAKA YOICHI: "Three-dimensional Integrated Circuit: Technology and Application Prospect", Microelectronics Journal, Vol. 20, No.s 1-2, 1989, pgs. 105 - 112.	Y
TDN	A202	SAKAMOTO KAJI: "Architecture des Circuits a Trois Dimension (Architecture of Three Dimensional Devices)", Bulletin of the Electrotechnical Laboratory, ISSN 0366-9092, Vol. 51, No. 1, 1987, pgs 16 - 29.	Y
TDN	A203	AKASAKA YOICHI: "Three-dimensional IC Trends", "Proceedings of the IEEE, Vol. 74, No. 12, 1986, Pgs. 1703 - 1714.	Y
TDN	A204	CARTER WILLIAM H.: "National Science Foundation (NSF) Forum on Optical Science and Engineering", Proceedings SPIE - The International Society for Optical Engineering, Vol. 2524, July 11 - 12 1995, (Article by N. Joverst titled "Manufacturable Multi-Material Integration Compound Semi-conductor Devices Bonded to Silicon Circuitry".	Y
TDN	A205	HAYASHI Y.: "A New Three Dimensional IC Fabrication Technology, Stacking Thin Film Dual-CMOS Layers", IEDM, 1991, pgs. 25.6.1 - 25.6.4.	Y
TDN	A206	REBER M.: "Benefits of Vertically Stacked Integrated Circuits for Sequential Logic", IEEE, 1996, pgs. 121-124.	Y
TDN	A207	STERN JON M.: "Design and Evaluation of an Epoxy Three-dimensional Multichip Module, IEEE Transactions on Components, Packaging, and Manufacturing Technology - Part B, Vol. 19, No. 1, February 1996, pgs 188-194.	Y
TDN	A208	BERTIN CLAUDE L.: "Evaluation of a Three-dimensional Memory Cube System", IEEE Transactions on Components, Hybrids, and Manufacturing Technology, Vol. 16, No. 8, December 1993, pgs. 1006 - 1011.	Y

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OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS				
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TN	A209	WATANABE HIDEHIRO: "Stacked Capacitor Cells for High-density Dynamic RAMs", IEDM, 1988, pgs. 600 - 603.		Y
TN	A210	WEB PAGE: "Stacked Memory Modules", IBM Technical Disclosure Bulletin, Vol. 38, No. 5, 1995.		Y
TN	A211	THAKUR SHASHIDHAR: "An Optimal Layer Assignment Algorithm for Minimizing Crosstalk for Three VHV Channel Routing", IEDM, 1995, pgs. 207 - 210.		Y
TN	A212	TERRIL ROB: "3D Packaging Technology Overview and Mass Memory Applications", IEDM, 1996, pgs. 347 - 355.		Y
TN	A213	INOUE Y.: "A Three-Dimensional Static RAM", IEEE Electron Device Letters, Vol. 7, No. 5, May 1986, pgs. 327 - 329.		Y
TN	A214	REBER M.: "Benefits of Vertically Stacked Integrated Circuits for Sequential Logic", IEDM, 1996, pgs. 121 - 124.		Y
TN	A215	KUROKAWA TAKAKAZU: "3-D VLSI Technology in Japan and an Example: A Syndrome Decoder for Double Error Correction", FGCS - Future, Generation, Computer, Systems", Vol. 4, No. 2, 1988, pgs. 145-155, Amsterdam, The Netherlands.		Y
TN	A216	MAKINIAK DAVID: "Vertical Integration of Silicon Allows Packaging of Extremely Dense System Memory In Tiny Volumes: Memory-chip Stacks Send Density Skyward", Electronic Design, No. 17, August 22, 1994, pgs. 69-75, Cleveland Ohio.		Y
TN	A217	SCHLAEPI H.P.: "nd Core Memories using Multiple Coincidence", IRE Transactions on Electronic Computers, June 1960, pgs 192 - 196.		Y
TN	A218	SCHLAEPI H.P.: "Session V: Information Storage Techniques", International Solid-State Circuits Conference, February 11, 1960, pgs. 54-55.		Y
TN	A219	YAMAZAKI K.: "Fabrication Technologies for Dual 4-KBIT Stacked SRAM", IEDM 16.8., 1986, pgs. 435-438.		Y
TN	A220	DE GRAAF C. et al.: "A Novel High-Density, Low-Cost Diode Programmable Read Only Memory," IEDM, beginning at page 189		Y

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TON	A221	PETER K. NAJI et al.: "A 256kb 3.0V 1T1MTJ Nonvolatile Magnetoresistive RAM," 2001 IEEE International Solid-State Circuits Conference, Digest of Technical Papers, ISSCC 2001/Session 7/Technology Directions: Advanced Technologies/7.6, February 6, 2001, pp. 122-123 (including enlargement of figures, totaling 9 pages), and associated Visual Supplement, pp. 94-95, 4040-405 (enlargements of slides submitted, totaling 25 pages)		Y
TON	A222	KIM C. HARDEE et al.: "A Fault-Tolerant 30 ns/375 mW 16K x 1 NMOS Static RAM," IEEE Journal of Solid-State Circuits, October 1981, Vol. SC-16, No. 5, pages 435-443		Y
TON	A223	TOSHIO WADA et al.: "A 15-ns 1024-Bit Fully Static MOS RAM," IEEE Journal of Solid-State Circuits, October 1978, Vol. SC-13, No. 5, pages 635-639		Y
TON	A224	CAMPERI-GINESTET C.: "Vertical Electrical Interconnection of Compound Semiconductor Thin-Film Devices to Underlying Silicon Circuitry", IEEE Photonics Technology Letters, Vol. 4, No. 9, September 1992, pgs. 1003-1006.		Y
TON	A225	PEIN HOWARD: "Performance of the 3-D PENCIL Flash EPROM Cell an Memory Array", IEEE Transactions on Electron Devices, Vol. 42, No. 11, November 1995, pgs. 1982-1991.		Y
TON	A226	Abstract LOMATCH S.: "Multilayered Josephson Junction Logic and Memory Devices", Proceedings of the SPIE-The International Society for Optical Engineering Vol. 2157, pgs. 332-343.		Y
TON	A227	Abstract LU N.C.C.: "Advanced Cell Structures for Dynamic RAMs", IEEE Circuits and Devices Magazine, Vol. 5, No. 1, January 1989, pgs. 27-36.		Y
TON	A228	Abstract SAKAMATO K.: "Architecture of Three Dimensional Devices", Journal: Bulletin of the Electrotechnical Laboratory, Vol. 51, No. 1, 1987, pgs. 16-29.		Y
TON	A229	Abstract "Wide Application of Low-Cost Associative Processing Associative Processing Seen", Electronic Engineering Times, August 26, 1996, pg. 43.		Y
TON	A230	Abstract "Interconnects & Packaging", Electronic Engineering Times, November 27, 1995, pg. 43.		Y
TON	A231	Abstract "Closing in on Gigabit DRAMs", Electronic Engineering Times, November 27, 1995, pg. 35.		Y
TON	A232	Abstract "Module Pact Pairs Cubic Memory with VisionTek", Semiconductor Industry & Business Survey, Vol. 17, No. 15, October 23, 1995.		Y

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TDN	A233	Abstract "Layers of BST Materials Push Toward 1Gbit DRAM", Electronics Times, October 19, 1995.		Y
TDN	A234	Abstract "Technologies Will Pursue Higher DRAM Densities", Electronic News (1991), December 4, 1994, pg. 12.		Y
TDN	A235	Abstract "Looking Diverse Storage", Electronic Engineering Times, October 31, 1994, pg. 44.		Y
TDN	A236	Abstract "Special Report: Memory Market Startups Cubic Memory: 3D Space Savers", Semiconductor Industry & Business Survey, Vol. 16, No. 13, September 12, 1994.		Y
TDN	A237	Abstract "Technique Boosts 3D Memory Density", Electronic Engineering Times, August 29, 1994, pg. 16.		Y
TDN	A238	Abstract "Memory Packs Poised 3D Use", Electronic Engineering Times, December 7, 1992, pg. 82.		Y
TDN	A239	Abstract "MCMs Hit the Road", Electronic Engineering Times, June 15, 1992, pg. 45.		Y
TDN	A240	Abstract "IEDM Ponders the 'Gigachip' Era", Electronic Engineering Times, January 20, 1992, pg. 33.		Y
TDN	A241	Abstract "Tech Watch: 1-Gbit DRAM in Sight", Electronic World News, December 16, 1991, pg. 20.		Y
TDN	A242	Abstract "MCMs Meld into Systems", Electronic Engineering Times, July 22, 1991, pg. 35.		Y
TDN	A243	Abstract "Systems EEs See Future in 3D", Electronic Engineering Times, September 24, 1990, pg. 37.		Y
TDN	A244	Patent Application, NISHIURA, US 2001/00054759 A1.		Y

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TDM	A245	Patent Application, FURUSAWA, US 2002/0024146 A1.	Y
TDM	A246	Patent Application, FUJIMOTO et al, US 2002/0027275 A1.	Y
TDM	A247	Patent Application, AKRAM, US 2002/0030262 A1.	Y
TDM	A248	Patent Application, AKRAM, US 2002/0030263 A1.	Y
TDM	A249	Patent Application, LEEDY, US 2001/0033030 A1.	Y

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¹ Unique citation designation number. ² See attached Kinds of U.S. Patent Documents. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Date Submitted: February 18, 2004 (use as many sheets as necessary)				Application Number	Unassigned
				Filing Date	February 18, 2004
				First Named Inventor	Kedar PATEL et al.
				Group Art Unit	Unassigned
				Examiner Name	Unassigned
Sheet	14	of	15	Attorney Docket Number	035905-0134

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
TJN	A250	6,110,278		Saxena	8/29/2000	
	A251	RE37,259	E	Ovshinsky	7/3/2001	
	A252	2001/0055838	A1	Walker, et al	12/27/2001	
TJN	A253	2002/0028541	A1	Lee, et al.	3/7/2002	

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ⁶
TJN	A254	"3D Chip-On-Chip Stacking," Semiconductor International, December 1991	Y
TJN	A255	RICHARD W. LAY: "TRW Develops Wireless Multiboard Interconnect System," Electronic Engineering Times, November 5, 1994	Y

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		Number	Kind Code ² (if known)			
[Signature]	A256	5,517,038		Maeda et al.	5/14/1996	
	A257	5,770,483		Kadosh et al.	6/23/1998	
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	A262	2003/0057435	A1	Walker	3/27/2003	

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